## REMARKS

The Applicant's representative has carefully reviewed and considered the Office Action mailed on April 29, 2002, and the references cited therewith. Claim 1 is amended, no claims are canceled, and no claims are added. As a result, claims 1-21 are now pending in this application.

### Rejections Under 35 U.S.C.§103

Claims 1-5, 8, 11, 13, 19, and 21 were rejected under 35 U.S.C.§103(a) as being unpatentable over Herrell et al. (U.S. Patent No. 6,191,479, hereinafter "Herrell") in view of Naito et al. (EP 0917165, hereinafter "NaitoEP"). The Applicant does not admit that Herrell or NaitoEP are prior art, and hereby reserves the right to swear behind both Herrell and NaitoEP as references. Nonetheless, since a *prima facie* case of obviousness has not been established, the Applicant respectfully traverses this rejection.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d (BNA) 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the *In re Fine* court:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

While it is not necessary that the cited references or prior art specifically suggest making the combination, there must be some teaching somewhere which provides the suggestion or motivation to combine prior art teachings and applies that combination to solve the same or similar problem which the claimed invention addresses. One of ordinary skill in the art will be presumed to know of any such teaching. (See, e.g., *In re Nilssen*, 851 F.2d 1401, 1403, 7 U.S.P.Q.2d (BNA) 1500, 1502 (Fed. Cir. 1988) and *In re Wood*, 599 F.2d 1032, 1037, 202 U.S.P.Q. (BNA) 171, 174 (C.C.P.A. 1979)). The requirement of a suggestion or motivation to combine references in a *prima facie* case of obviousness is emphasized in the Federal Circuit opinion, *In re Sang Su Lee*, 277 F.3d 1338; 61 U.S.P.Q.2D 1430 (Fed. Cir. 2002), which indicates that the motivation must be supported by evidence in the record.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 U.S.P.Q. (BNA) 543, 551 (Fed. Cir. 1985). References must be considered in their entirety, including parts that teach away from the claims. See § MPEP 2141.02.

In this case, neither of the references disclose a substrate, and Herrell also does not disclose a third conductive layer, a third insulator layer, nor a plurality of vias extending downwardly through the third insulator layer. Further, there is no evidence in the record supporting a motivation to combine the references. Finally, the references teach away from such a combination, as combining the references would destroy the intended purpose of the invention.

First, as noted in previous responses, NaitoEP does not disclose "a substrate", as claimed by the Applicant in independent claims 1, 11, and 19. Herrell also does not disclose a substrate. While the Office Action asserts that element 12 of Herrell is a "substrate", no discussion of element 12 occurs in the text of Herrell. Further, the numerous references to a substrate (not shown) in Herrel are made with respect to an associated integrated circuit, and not for a capacitor. See, for example, Herrell, Col. 3, lines 43-48. In fact, Herrell is careful to differentiate the identical, corresponding element to element 12 (i.e., element 22 in FIG. 2) by describing it as an insulator, and not as a substrate. See Herrell, Col. 8, line 63. Also, as admitted in the Office Action, Herrell does not disclose a third conductive layer, nor a third

insulator layer, nor a plurality of vias downwardly extending through the third insulator layer, as claimed by the Applicant in independent claims 1, 11, and 19. See Paper 11, pg. 3, lines 7-10.

For these reasons, it is clear that neither Herrell nor NaitoEP teach or suggest the use of a substrate as claimed by the Applicant. Therefore, neither of these references, separately, or in combination, can teach or suggest the claimed subject matter.

Second, to supply the admitted defects of Herrell (i.e., lack of third conductive and insulator layers, and vias extending downwardly therethrough), the Office Action states "it would have been obvious ...to add a third conductive layer and a third insulator layer to the capacitor of Herrell et al., since such a modification would improve the capacitance of the system".

Although the Office Action asserts Herrell teaches "the number of conductive layers is not limited", the Applicant was unable to find where this was indicated in the reference. Herrell does teach the use of additional electrodes, but only by breaking up larger electrodes into smaller, serial electrodes forming a part of the same layer. Herrell, Col. 9, line 59 - Col. 10, line 4. Herrell never teaches more than two conductive layers formed one over the other, and in fact urges the use of additional decoupling capacitors according to his design to accommodate additional, corresponding power supply voltages. This is supported by Herrell's statement that "larger numbers of power supply voltages may be employed with ... the addition of corresponding metal layers in decoupling capacitor configurations." Herrell, Col. 10, lines 40-43.

The assertion made in the Office Action also overlooks the fact that Herrell has already provided a specific solution to this problem. Herrell discusses a decoupling capacitor designed to take advantage of large surface areas and to reduce inductive impedance by placing the capacitor in close physical proximity to the decoupled circuitry. See Herrell, Col. 4, lines 28-31. As noted by Herrell, "... the inductive impedance of intervening portions of the power supply loop circuit (e.g. of chip and package-level interconnect features such as vias ... etc.) typically limits the efficacy of off-chip decoupling capacitors." See Herrell, Col. 2, lines 12-19. Even capacitors integrated with the circuit package fail in this respect. See Herrell, Col. 2, lines 33-40. Therefore, merely adding extra conductive layers, which *increases* inductance, and fails to take advantage of available surface area using a multiplicity of shorter connections to the adjacent

circuitry, is antithetical to the invention of Herrell. See Herrell, Col. 6, lines 25-30. If a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed invention. *In re Gordon*, 221 USPQ 1125 (Fed. Cir. 1984), and M.P.E.P. § 2143.01. Since there is no support to combine the references in the record, the requirements of *In re Sang Su Lee* are not satisfied.

Finally, Herrell and NaitoEP both teach away from combining the references. Simply adding an additional conductive layer from NaitoEP to Herrell's invention would provide the opposite effect of that desired. That is, instead of decreasing inductance and minimizing the distance between the capacitor to the decoupled circuitry, as desired by Herrell, the inductance would be increased, as would the distance between the capacitor and the circuitry. Such an addition also defeats the fundamental objective of NaitoEP, which teaches a multilayer capacitor having paired connection portions which serve to reduce magnetic flux. NaitoEP, Pg. 7, para. 62. Adding a single conductive layer, an insulator, and corresponding connections would result in *unpaired* connection portions, *increasing* magnetic flux.

Thus, neither of the references disclose a substrate as claimed by the Applicant. Further, there is no evidence in the record supporting a specific motivation to combine the Herrell and NaitoEP references, as required by *In re Sang Su Lee*. Finally, the references teach away from such a combination, and combining the references would destroy the intended purpose of the invention.

Since the references can not be combined to provide the claimed invention, since there is no motivation to combine the references (the combination destroys the purpose of the invention), and since the references teach away from such a combination, a *prima facie* case of obviousness has not been established with respect to independent claims 1, 11, and 19. This conclusion applies with even greater force with respect to the dependent claims, since each one includes additional, patentable features over those delineated in the independent claims. If an independent claim is nonobvious under 35 USC § 103, then any claim depending therefrom is nonobvious. See M.P.E.P. § 2143.03. Therefore, the Applicant respectfully requests reconsideration and withdrawal of the rejection under § 103.

## Allowable Subject Matter

Claims 9-10, and 14-18 have been allowed. Claims 6-7, 12, and 20 have been objected to as being dependent upon a rejected base claim, but are allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

## CONCLUSION

The Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 8 day of July, 2002.

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Name

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Signature

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**Clean Version of Pending Claims**

MULTI-LAYER CHIP CAPACITOR
Applicant: Larry Eugene Mosley
Serial No.: 09/537,274

D1

1. (Twice Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

SUB E1

2. The multi layer integrated circuit capacitor of claim 1 further comprising a plurality of controlled collapse chip connection (C4) lands fabricated on and contacting the third insulator layer and in electrical contact with the plurality of conductive vias.

3. The multi layer integrated circuit capacitor of claim 2 wherein the C4 lands are fabricated in staggered columns in a plan view.

4. The multi layer integrated circuit capacitor of claim 1 wherein at least one of the conductive layers comprise a metal material and at least one of the insulator layers comprise $BaSrTiO_3$.

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5. The multi layer integrated circuit capacitor of claim 4 wherein at least one of the conductive layers are fabricated from a copper.

6. The multi layer integrated circuit capacitor of claim 1 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias.

7. The multi layer integrated circuit capacitor of claim 1 wherein the second and third conductive layers are fabricated in a plurality of strips, such that a surface area of the second conductive layer is less than a surface area of the first conductive layer and a surface area of the third conductive layer is less than the surface area of the second conductive layer.

8. The multi layer integrated circuit capacitor of claim 1 wherein some of the plurality of conductive vias pass through the second conductive layer without forming an electrical connection with the second conductive layer.

SUB E1

9. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer, the second conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer;

a second insulator layer located over the second conductive layer;

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a third conductive layer located over the second insulator layer, the third conductive layer being fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the third conductive layer;

a second plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the second conductive layer; and

a third plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first conductive layer.

10. The multi layer integrated circuit capacitor of claim 9 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect at least one of the pluralities of conductive vias.

11. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer;

a first plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, the second insulator layer, the second conductive layer and the

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first insulator layer to provide electrical interconnection to the first and third conductive layers; and

a second plurality of conductive vias downwardly extending through the third insulator layer, the third conductive layer, and the second insulator layer to provide electrical interconnection to the second conductive layer.

12. The multi layer integrated circuit capacitor of claim 11 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect at least one of the pluralities of conductive vias.

13. The multi layer integrated circuit capacitor of claim 11 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise $BaSrTiO_3$.

14. A circuit board assembly comprising:

a circuit board having a pair of supply voltage interconnect lines;

a first integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines; and

a second integrated circuit die mounted on the circuit board and electrically connected to the supply voltage interconnect lines, the second integrated circuit die comprising a capacitor having:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

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a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers.

D ~~15~~. The circuit board assembly of claim 14 wherein the second integrated circuit die comprises a plurality of controlled collapse chip connection (C4) lands that are electrically connected to the plurality of conductive vias and the supply voltage interconnect lines.

16. The circuit board assembly of claim 14 wherein the first integrated circuit package is a processor circuit.

17. The circuit board assembly of claim 14 wherein at least one of the conductive layers comprise a metal material and wherein at least one of the insulator layers comprise $BaSrTiO_3$.

18. The circuit board assembly of claim 14 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of plurality of conductive vias.

19. A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

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a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductive layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second, and third conductive layers, the plurality of conductive vias further extending through the substrate to provide electrical interconnection to both a top surface and a bottom surface of the integrated circuit capacitor.

20. The multi layer integrated circuit capacitor of claim 19 further comprising a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias.

21. The multi layer integrated circuit capacitor of claim 1 wherein each of the conductor layers comprise a metal material and wherein each of the insulator layers comprise $BaSrTiO_3$.